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10/084,970	03/01/2002	Takahiro Koishi	Q68781	2189

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,970	KOISHI, TAKAHIRO	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 4/11/2002.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 01 March 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/11/2002.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iseya (JP 63246049 A) in view of Sakai et al. (US 6,005,869) and Fredrickson (US 5,757,826).

As per claim 1, Iseya teaches a transmission data loss detection method in a data transmission system in which a sending unit deblocks parent data into pieces of unit data and sends each piece of unit data in sequence, and a receiving unit blocks each piece of received unit data to reconstruct the parent data, comprising the steps of: calculating an ECC for a data sequence having an ID added corresponding to each piece of unit data in the sending unit; sending send data having each piece of unit data with the added ECC; returning each ID to the corresponding expected ID and resending from the unit data corresponding to the expected ID in case of receiving a resend request including an expected ID from the receiving unit; and blocking the corresponding unit data in the case where the ECC in the receive data and the expected ECC are the same (abstract, Iseya).

However Iseya does not explicitly teach that the sending unit does not include ID in the send data.

Sakai et al. in an analogous art teach that each station transfers a data packet, which it has by using the transmission band reserved by the token packet, wherein the data packet includes no ID information.

In accordance with the thirtieth aspect, a token packet containing ID information is sent to reserve transmission bandwidth and a data packet, which is sent after it, contains no ID information (col. 8, lines 15-21, Sakai et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Sakai et al. by including additionally that the sending unit does not include ID in the send data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the sending unit not including ID in the send data would provide the opportunity to increase the information data transmission density over the transmission medium and prevent unwanted transmission overhead.

Iseya also does not explicitly teach receiving the send data as receive data and calculating the expected ECC for the data sequence having an expected ID added corresponding to each piece of unit data in the receive data in the receiving unit; comparing the ECC in the receive data and the expected ECC; issuing the resend request including the expected ID to the sending unit in the case where the ECC in the receive data and the expected ECC are not the same.

However Fredrickson in an analogous art teaches that error detection and correction techniques typically rely on some form of appended redundancy information to protect data blocks from errors during transmission through a noisy communication or recording channel. This appended redundancy is generated from, and thus dependent upon, the precise bit pattern that forms the data block to be protected. The integrity of the data at a receiving end is checked by regenerating the redundancy from the received data block (using the same coding algorithm used to generate the redundancy at the transmission end) and then comparing the regenerated redundancy with the originally appended redundancy. After this comparison, if data errors are determined to be present, a request can be made to re-transmit or re-read the data (col. 1, lines 26-40, Fredrickson).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Fredrickson by including additionally, receiving the send data as receive data and calculating the expected ECC for the data sequence having an expected

ID added corresponding to each piece of unit data in the receive data in the receiving unit; comparing the ECC in the receive data and the expected ECC; issuing the resend request including the expected ID to the sending unit in the case where the ECC in the receive data and the expected ECC are not the same. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect data transmission errors in the receive data and retransmit the data if an error is detected.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iseya (JP 63246049 A), Sakai et al. (US 6,005,869) and Fredrickson (US 5,757,826) as applied to claim 1 above, and further in view of Iwamoto et al. (US 6,611,652 B1).

As per claim 2, Iseya, Sakai et al. and Fredrickson substantially teach the claimed invention described in claim 1 (as rejected above).

However Iseya, Sakai et al. and Fredrickson do not explicitly teach specifically that the ID is incremented cyclically in a predetermined range.

Iwamoto et al. in an analogous art teach that the cyclic ID is incremented in units of GOPs and indicates the order of the audio and/or video data for every eight GOPs (col. 31, lines 27-29, Iwamoto et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Iwamoto et al. by including additionally that the ID is incremented cyclically in a predetermined range.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that incrementing the ID cyclically in a predetermined range would provide the opportunity to identify the data unit and resend the data unit if the received data unit has an error.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iseya (JP 63246049 A) in view of Sakai et al. (US 6,005,869), Fredrickson (US 5,757,826) and Butler et al. (US 4,654,654).

As per claim 3, Iseya teaches a transmission data loss detection system, comprising a sending unit for deblocking parent data into each piece of unit data and sending each piece of unit data in sequence; and a receiving unit for blocking each piece of received unit data to reconstruct the parent data, wherein the

sending unit includes a deblocking circuit for deblocking parent data into each piece of unit data, a deblocking buffer for storing each piece of unit data deblocked by the deblocking circuit, an ID-generating circuit for generating an ID corresponding to each piece of unit data, an ECC-generating circuit for generating an ECC for the data sequence having the unit data and the ID, an ID-generating circuit for generating an expected ID corresponding to each piece of unit data in the receive data, a blocking buffer for storing the corresponding unit data in the case where the ECC and the expected ECC in the receive data are the same and a blocking circuit for blocking all the unit data to reconstruct the parent data when all the unit data constituting the parent data is stored in the blocking buffer (abstract, Iseya).

However Iseya does not explicitly teach that the send-data buffer does not include ID in the send data sequence.

Sakai et al. in an analogous art teach that each station transfers a data packet, which it has by using the transmission band reserved by the token packet, wherein the data packet includes no ID information.

In accordance with the thirtieth aspect, a token packet containing ID information is sent to reserve transmission bandwidth and a data packet, which is sent after it, contains no ID information (col. 8, lines 15-21, Sakai et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Sakai et al. by including additionally that the send-data buffer does not include ID in the send data sequence.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the send-data buffer not including ID in the send data sequence would provide the opportunity to increase the information data transmission density over the transmission medium and prevent unwanted transmission overhead.

Iseya also does not explicitly teach a send-data buffer for storing the data sequence having the unit data and the ECC, and a sending/receiving circuit for sending the data sequence stored in the send-data buffer to a transmission path as send data; and the receiving unit includes a sending/receiving circuit for receiving the send data from the transmission path as receive data, a receive-data buffer for storing the receive data received by the sending/receiving circuit.

However Butler et al. in an analogous art teach the host processor 111 in this system does not directly control the sending of packets to the data network medium. It communicates various types of requests to the network interface 100, including requests to send a packet stored in a block of memory, called a transmit buffer, in memory 116 of the host processor 111 or in shared memory 112 (transmit buffer 330 in figure 6, col. 5, lines 45 – 51, Butler et al.). Butler et al. teach that transmit circuit interface block 161 and receive circuit interface block 151 are connected to the data network medium 110 and the transmit control 164 and receive control 152, respectively (figure 2, col. 7, lines 3-6, Butler et al.). Butler et al. teach that the receive port number is later used by interface processor 153 to find the address of a block of memory, called a receive buffer, where the packet data of the packet is to be stored (receive buffer 360 in figure 6, col. 8, lines 60-63, Butler et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Butler et al. by including additionally a send-data buffer for storing the data sequence having the unit data and the ECC, and a sending/receiving circuit for sending the data sequence stored in the send-data buffer to a transmission path as send data; and the receiving unit includes a sending/receiving circuit for receiving the send data from the transmission path as receive data, a receive-data buffer for storing the receive data received by the sending/receiving circuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to temporarily store the data to be transmitted in the send-data buffer and received data in the receive-data buffer so that the data can be processed by the sending circuit and receiving circuit respectively. The transmission and receiving circuits are used to transmit the data on the transmission medium and receive the send data from the transmission medium respectively.

Iseya also does not explicitly teach an ECC-calculating circuit for calculating an expected ECC for the data sequence having the unit data and the expected ID in the receive data, a compare circuit for comparing the ECC and the expected ECC in the receive data, a resend-request circuit for issuing a

resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same.

However Fredrickson in an analogous art teaches that error detection and correction techniques typically rely on some form of appended redundancy information to protect data blocks from errors during transmission through a noisy communication or recording channel. This appended redundancy is generated from, and thus dependent upon, the precise bit pattern that forms the data block to be protected. The integrity of the data at a receiving end is checked by regenerating the redundancy from the received data block (using the same coding algorithm used to generate the redundancy at the transmission end) and then comparing the regenerated redundancy with the originally appended redundancy. After this comparison, if data errors are determined to be present, a request can be made to re-transmit or re-read the data (col. 1, lines 26-40, Fredrickson).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Fredrickson by including additionally, an ECC-calculating circuit for calculating an expected ECC for the data sequence having the unit data and the expected ID in the receive data, a compare circuit for comparing the ECC and the expected ECC in the receive data, a resend-request circuit for issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect data transmission errors in the receive data and retransmit the data if an error is detected.

6. Claims 4, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iseya (JP 63246049 A) in view of Sakai et al. (US 6,005,869) and Butler et al. (US 4,654,654).

As per claim 4, Iseya teaches a sending unit comprising: a deblocking circuit for deblocking parent data into each piece of unit data; a deblocking buffer for storing each piece of unit data deblocked by the deblocking circuit; an ID-generating circuit for generating an ID corresponding to each piece of unit data; an ECC-generating circuit for generating an ECC for the data sequence having the unit data and the corresponding ID (abstract, Iseya).

However Iseya does not explicitly teach that the send-data buffer does not include ID in the send data sequence.

Sakai et al. in an analogous art teach that each station transfers a data packet, which it has by using the transmission band reserved by the token packet, wherein the data packet includes no ID information.

In accordance with the thirtieth aspect, a token packet containing ID information is sent to reserve transmission bandwidth and a data packet, which is sent after it, contains no ID information (col. 8, lines 15-21, Sakai et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Sakai et al. by including additionally that the send-data buffer does not include ID in the send data sequence.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the send-data buffer not including ID in the send data sequence would provide the opportunity to increase the information data transmission density over the transmission medium and prevent unwanted transmission overhead.

Iseya also does not explicitly teach a send-data buffer for storing the data sequence having the unit data and the ECC; and a sending/receiving circuit for sending the data sequence stored in the send-data buffer to a transmission path as send data.

However Butler et al. in an analogous art teach the host processor 111 in this system does not directly control the sending of packets to the data network medium. It communicates various types of requests to the network interface 100, including requests to send a packet stored in a block of memory, called a transmit buffer, in memory 116 of the host processor 111 or in shared memory 112 (transmit buffer 330 in figure 6, col. 5, lines 45 – 51, Butler et al.). Butler et al. teach that transmit circuit interface block 161 and receive circuit interface block 151 are connected to the data network medium 110 and the transmit control 164 and receive control 152, respectively (figure 2, col. 7, lines 3-6, Butler et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Butler et al. by including additionally a send-data

buffer for storing the data sequence having the unit data and the ECC; and a sending/receiving circuit for sending the data sequence stored in the send-data buffer to a transmission path as send data.
This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to temporarily store the data to be transmitted in the send-data buffer so that the data can be processed by the sending circuit. The transmission and receiving circuits are used to transmit the data on the transmission medium and receive the send data from the transmission medium respectively.

- As per claim 7, Iseya, Sakai et al. and Butler et al. teach the additional limitations.

Iseya teaches a sending unit comprising: deblocking means for deblocking parent data into each piece of unit data; deblocking buffer means for storing each piece of unit data deblocked by the deblocking means; ID-generating means for generating an ID corresponding to each piece of unit data; ECC-generating means for generating an ECC for the data sequence having the unit data and ID (abstract, Iseya).
Sakai et al. teach that the send-data buffer does not include ID in the send data sequence (col. 8, lines 15-21, Sakai et al.).
Butler et al. teach send-data buffer means for storing the data sequence having the unit data and the ECC; and sending/receiving means for sending the data sequence stored in the send-data buffer to a transmission path as send data (figure 2, transmit buffer 330 in figure 6, col. 5, lines 45 – 51, col. 7, lines 3-6, Butler et al.).

7. Claims 5, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iseya (JP 63246049 A) in view of Fredrickson (US 5,757,826) and Butler et al. (US 4,654,654).

As per claim 5, Iseya teaches an ID-generating circuit for generating an expected ID corresponding to each piece of unit data in the receive data; a blocking buffer for storing the corresponding unit data in the case where the ECC and the expected ECC in the receive data are the same; and a blocking circuit for blocking all the unit data to reconstruct the parent data when all the unit data constituting the parent data is stored in the blocking buffer (abstract, Iseya).

However Iseya does not explicitly teach the specific use of a receiving unit comprising: a sending/receiving circuit for receiving send data from a transmission path as receive data and a receive-data buffer for storing the receive data received by the sending/receiving circuit.

However Butler et al. in an analogous art teach transmit circuit interface block 161 and receive circuit interface block 151 are connected to the data network medium 110 and the transmit control 164 and receive control 152, respectively (figure 2, col. 7, lines 3-6, Butler et al.). Butler et al. teach that the receive port number is later used by interface processor 153 to find the address of a block of memory, called a receive buffer, where the packet data of the packet is to be stored (receive buffer 360 in figure 6, col. 8, lines 60-63, Butler et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Butler et al. by including additionally a receiving unit comprising: a sending/receiving circuit for receiving send data from a transmission path as receive data and a receive-data buffer for storing the receive data received by the sending/receiving circuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to temporarily store the received data in the receive-data buffer so that the data can be processed by the receiving circuit. The transmission and receiving circuits are used to transmit the data on the transmission medium and receive the send data from the transmission medium respectively.

Iseya also does not explicitly teach the specific use of an ECC-calculating circuit for calculating an expected ECC for the data sequence having each piece of unit data and the expected ID in the receive data; a compare circuit for comparing the ECC and the expected ECC in the receive data; a resend-request circuit for issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same.

However Fredrickson in an analogous art teaches that error detection and correction techniques typically rely on some form of appended redundancy information to protect data blocks from errors during transmission through a noisy communication or recording channel. This appended redundancy is generated from, and thus dependent upon, the precise bit pattern that forms the data block to be

protected. The integrity of the data at a receiving end is checked by regenerating the redundancy from the received data block (using the same coding algorithm used to generate the redundancy at the transmission end) and then comparing the regenerated redundancy with the originally appended redundancy. After this comparison, if data errors are determined to be present, a request can be made to re-transmit or re-read the data (col. 1, lines 26-40, Fredrickson).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Fredrickson by including an additional step of using an ECC-calculating circuit for calculating an expected ECC for the data sequence having each piece of unit data and the expected ID in the receive data; a compare circuit for comparing the ECC and the expected ECC in the receive data; a resend-request circuit for issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect data transmission errors in the receive data and retransmit the data if an error is detected.

- As per claim 8, Iseya, Fredrickson and Butler et al. teach the additional limitations.

Butler et al. teach a receiving unit comprising: sending/receiving means for receiving the send data from a transmission path as receive data and receive-data buffer means for storing the receive data received by the sending/receiving means (figure 2, receive buffer 360 in figure 6, col. 7, lines 3-6, col. 8, lines 60-63, Butler et al.).

Iseya teaches ID-generating means for generating an expected ID corresponding to each piece of unit data in the receive data; blocking buffer means for storing the corresponding unit data in the case where the ECC and the expected ECC in the receive data are the same; and blocking means for blocking all the unit data to reconstruct the parent data when all the unit data constituting the parent data is stored in the blocking buffer (abstract, Iseya).

Fredrickson teaches ECC-calculating means for calculating an expected ECC for the data sequence having each piece of unit data and the expected ID in the receive data; compare means for comparing the

ECC and the expected ECC in the receive data and resend-request means for issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same (col. 1, lines 26-40, Fredrickson).

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iseya (JP 63246049 A) in view of Sakai et al. (US 6,005,869), Fredrickson (US 5,757,826) and Butler et al. (US 4,654,654).

As per claim 6, Iseya teaches a transmission data loss detection system, comprising: a sending unit for deblocking parent data into each piece of unit data and sending each piece of unit data in sequence; and a receiving unit for blocking each piece of received unit data to reconstruct the parent data, wherein the sending unit includes a deblocking means for deblocking parent data into each piece of unit data, a deblocking buffer means for storing each piece of unit data deblocked by the deblocking means, an ID-generating means for generating an ID corresponding to each piece of unit data, an ECC-generating means for generating an ECC for the data sequence having the unit data and the ID, an ID-generating means for generating an expected ID corresponding to each piece of unit data in the receive data, a blocking buffer means for storing the corresponding unit data in the case where the ECC and the expected ECC in the receive data are the same, and a blocking means for blocking all the unit data to reconstruct the parent data when all the unit data constituting the parent data is stored in the blocking buffer (abstract, Iseya).

However Iseya does not explicitly teach that the send-data buffer does not include ID in the send data sequence.

Sakai et al. in an analogous art teach that each station transfers a data packet, which it has by using the transmission band reserved by the token packet, wherein the data packet includes no ID information.

In accordance with the thirtieth aspect, a token packet containing ID information is sent to reserve transmission bandwidth and a data packet, which is sent after it, contains no ID information (col. 8, lines 15-21, Sakai et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Sakai et al. by including additionally that the send-data buffer does not include ID in the send data sequence.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the send-data buffer not including ID in the send data sequence would provide the opportunity to increase the information data transmission density over the transmission medium and prevent unwanted transmission overhead.

Iseya also does not explicitly teach the specific use of a send-data buffer means for storing the data sequence having the unit data and the ECC, and a sending/receiving means for sending the data sequence stored in the send-data buffer to a transmission path as send data; and the receiving unit includes a sending/receiving means for receiving the send data from the transmission path as receive data and a receive-data buffer means for storing the receive data received by the sending/receiving means.

However Butler et al. in an analogous art teach the host processor 111 in this system does not directly control the sending of packets to the data network medium. It communicates various types of requests to the network interface 100, including requests to send a packet stored in a block of memory, called a transmit buffer, in memory 116 of the host processor 111 or in shared memory 112 (transmit buffer 330 in figure 6, col. 5, lines 45 – 51, Butler et al.). Butler et al. teach that transmit circuit interface block 161 and receive circuit interface block 151 are connected to the data network medium 110 and the transmit control 164 and receive control 152, respectively (figure 2, col. 7, lines 3-6, Butler et al.). Butler et al. teach that the receive port number is later used by interface processor 153 to find the address of a block of memory, called a receive buffer, where the packet data of the packet is to be stored (receive buffer 360 in figure 6, col. 8, lines 60-63, Butler et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Butler et al. by including additionally a send-data buffer means for storing the data sequence having the unit data and the ECC, and a sending/receiving means for sending the data sequence stored in the send-data buffer to a transmission path as send data; and the receiving unit includes a sending/receiving means for receiving the send data from the transmission path as receive data and a receive-data buffer means for storing the receive data received by the sending/receiving means.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to temporarily store the data to be transmitted in the send-data buffer and received data in the receive-data buffer so that the data can be processed by the sending circuit and receiving circuit respectively. The transmission and receiving circuits are used to transmit the data on the transmission medium and receive the send data from the transmission medium respectively.

Iseya also does not explicitly teach the specific use of an ECC-calculating means for calculating an expected ECC for the data sequence having the unit data and the expected ID in the receive data, a compare means for comparing the ECC and the expected ECC in the receive data and a resend-request means for issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same.

However Fredrickson in an analogous art teaches that error detection and correction techniques typically rely on some form of appended redundancy information to protect data blocks from errors during transmission through a noisy communication or recording channel. This appended redundancy is generated from, and thus dependent upon, the precise bit pattern that forms the data block to be protected. The integrity of the data at a receiving end is checked by regenerating the redundancy from the received data block (using the same coding algorithm used to generate the redundancy at the transmission end) and then comparing the regenerated redundancy with the originally appended redundancy. After this comparison, if data errors are determined to be present, a request can be made to re-transmit or re-read the data (col. 1, lines 26-40, Fredrickson).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Fredrickson by including additionally, an ECC-calculating means for calculating an expected ECC for the data sequence having the unit data and the expected ID in the receive data, a compare means for comparing the ECC and the expected ECC in the receive data and a resend-request means for issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect data transmission errors in the receive data and retransmit the data if an error is detected.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iseya (JP 63246049 A) in view of Sakai et al. (US 6,005,869), Fredrickson (US 5,757,826), Butler et al. (US 4,654,654) and Sitterley (US 6,275,966 B1).

As per claim 9, Iseya teaches deblocking parent data into each piece of unit data, storing each piece of deblocked unit data by the deblocking means, generating an ID for each piece of unit data, generating an ECC for the data sequence having the unit data and the ID, storing the data sequence having the unit data and the ECC, generating an expected ID corresponding to each piece of unit data in the receive data, storing the unit data in the case where the ECC and the expected ECC in the receive data are the same, blocking all the unit data to reconstruct the parent data when all the unit data constituting the parent data is stored in blocking buffer means (abstract, Iseya).

However Iseya does not explicitly teach that the send-data sequence does not include the ID for the unit data.

Sakai et al. in an analogous art teach that each station transfers a data packet, which it has by using the transmission band reserved by the token packet, wherein the data packet includes no ID information.

In accordance with the thirtieth aspect, a token packet containing ID information is sent to reserve transmission bandwidth and a data packet, which is sent after it, contains no ID information (col. 8, lines 15-21, Sakai et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Sakai et al. by including additionally that the send-data sequence does not include the ID for the unit data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the send-data sequence not including the ID for the unit data would provide the opportunity to increase the information data transmission density over the transmission medium and prevent unwanted transmission overhead.

Iseya also does not explicitly teach sending the data sequence stored in the send-data buffer means to a transmission path as send data; and steps to be executed on a receiving computer, including receiving the send data from a transmission path as receive data, storing the receive data received by the sending/receiving means.

However Butler et al. in an analogous art teach the host processor 111 in this system does not directly control the sending of packets to the data network medium. It communicates various types of requests to the network interface 100, including requests to send a packet stored in a block of memory, called a transmit buffer, in memory 116 of the host processor 111 or in shared memory 112 (transmit buffer 330 in figure 6, col. 5, lines 45 – 51, Butler et al.). Butler et al. teach that transmit circuit interface block 161 and receive circuit interface block 151 are connected to the data network medium 110 and the transmit control 164 and receive control 152, respectively (figure 2, col. 7, lines 3-6, Butler et al.). Butler et al. teach that the receive port number is later used by interface processor 153 to find the address of a block of memory, called a receive buffer, where the packet data of the packet is to be stored (receive buffer 360 in figure 6, col. 8, lines 60-63, Butler et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Butler et al. by including an additional step of sending the data sequence stored in the send-data buffer means to a transmission path as send data; and steps to be executed on a receiving computer, including receiving the send data from a transmission path as receive data, storing the receive data received by the sending/receiving means.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to temporarily store the data to be transmitted in the send-data buffer and received data in the receive-data buffer so that the data can be processed by the sending circuit and receiving circuit respectively. The transmission and receiving circuits are used to transmit the data on the transmission medium and receive the send data from the transmission medium respectively.

Iseya also does not explicitly teach calculating an expected ECC for the data sequence having each piece of unit data and the expected ID in the receive data, comparing the ECC and the expected ECC in

the receive data, and issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same.

However Fredrickson in an analogous art teaches that error detection and correction techniques typically rely on some form of appended redundancy information to protect data blocks from errors during transmission through a noisy communication or recording channel. This appended redundancy is generated from, and thus dependent upon, the precise bit pattern that forms the data block to be protected. The integrity of the data at a receiving end is checked by regenerating the redundancy from the received data block (using the same coding algorithm used to generate the redundancy at the transmission end) and then comparing the regenerated redundancy with the originally appended redundancy. After this comparison, if data errors are determined to be present, a request can be made to re-transmit or re-read the data (col. 1, lines 26-40, Fredrickson).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Fredrickson by including an additional step of calculating an expected ECC for the data sequence having each piece of unit data and the expected ID in the receive data, comparing the ECC and the expected ECC in the receive data, and issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect data transmission errors in the receive data and retransmit the data if an error is detected.

Iseya also does not explicitly teach a computer program for driving a computer to execute steps in a transmission data loss detection system, the steps comprising steps to be executed on a sending computer.

However Sitterley in an analogous art teaches the computer program instructions may be executed by a processor to cause a series of operational steps to be performed by the processor to produce a computer implemented process such that the instructions which execute on the processor provide steps for implementing the functions specified in the flowchart block or blocks (col. 7, lines 15-20, Sitterley).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Sitterley by including an additional step of using a computer program for driving a computer to execute steps in a transmission data loss detection system, the steps comprising steps to be executed on a sending computer.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to execute the process steps faster and accurately.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iseya (JP 63246049 A) in view of Sakai et al. (US 6,005,869), Butler et al. (US 4,654,654) and Sitterley (US 6,275,966 B1).

As per claim 10, Iseya teaches deblocking parent data into each piece of unit data; storing each deblocked unit data; generating an ID corresponding to each piece of unit data, generating an ECC for the data sequence having the unit data and the ID (abstract, Iseya).

However Iseya does not explicitly teach that the send-data sequence does not include the ID for the unit data.

Sakai et al. in an analogous art teach that each station transfers a data packet, which it has by using the transmission band reserved by the token packet, wherein the data packet includes no ID information.

In accordance with the thirtieth aspect, a token packet containing ID information is sent to reserve transmission bandwidth and a data packet, which is sent after it, contains no ID information (col. 8, lines 15-21, Sakai et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Sakai et al. by including additionally that the send-data sequence does not include the ID for the unit data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the send-data sequence not including the ID for the unit data would provide the opportunity to increase the information data transmission density over the transmission medium and prevent unwanted transmission overhead.

Iseya also does not explicitly teach the specific use of a send-data buffer means for storing the data sequence having the unit data and the ECC; and sending the data sequence stored in the send-data buffer means to a transmission path as send data.

However Butler et al. in an analogous art teach the host processor 111 in this system does not directly control the sending of packets to the data network medium. It communicates various types of requests to the network interface 100, including requests to send a packet stored in a block of memory, called a transmit buffer, in memory 116 of the host processor 111 or in shared memory 112 (transmit buffer 330 in figure 6, col. 5, lines 45 – 51, Butler et al.). Butler et al. teach that transmit circuit interface block 161 and receive circuit interface block 151 are connected to the data network medium 110 and the transmit control 164 and receive control 152, respectively (figure 2, col. 7, lines 3-6, Butler et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Butler et al. by including additionally a send-data buffer means for storing the data sequence having the unit data and the ECC; and sending the data sequence stored in the send-data buffer means to a transmission path as send data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to temporarily store the data to be transmitted in the send-data buffer so that the data can be processed by the sending circuit. The transmission and receiving circuits are used to transmit the data on the transmission medium and receive the send data from the transmission medium respectively.

Iseya also does not explicitly teach a computer program for driving a sending computer to execute steps in a transmission data loss detection system

However Sitterley in an analogous art teaches the computer program instructions may be executed by a processor to cause a series of operational steps to be performed by the processor to produce a computer implemented process such that the instructions which execute on the processor provide steps for implementing the functions specified in the flowchart block or blocks (col. 7, lines 15-20, Sitterley).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Sitterley by including an additional step of using a

computer program for driving a sending computer to execute steps in a transmission data loss detection system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to execute the process steps faster and accurately.

11. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iseya (JP 63246049 A) in view of Fredrickson (US 5,757,826), Butler et al. (US 4,654,654) and Sitterley (US 6,275,966 B1).

As per claim 11, Iseya teaches generating an expected ID for each piece of unit data in the receive data; storing the corresponding unit data in the case where the ECC and the expected ECC in the receive data are the same, and blocking all the unit data to reconstruct the parent data when all the unit data constituting the parent data is stored in blocking buffer means (abstract, Iseya).

However Iseya does not explicitly teach receiving send data from a transmission path as receive data and storing the receive data received by the sending/receiving means.

Butler et al. in an analogous art teach transmit circuit interface block 161 and receive circuit interface block 151 are connected to the data network medium 110 and the transmit control 164 and receive control 152, respectively (figure 2, col. 7, lines 3-6, Butler et al.). Butler et al. teach that the receive port number is later used by interface processor 153 to find the address of a block of memory, called a receive buffer, where the packet data of the packet is to be stored (receive buffer 360 in figure 6, col. 8, lines 60-63, Butler et al.).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Butler et al. by including an additional step of receiving send data from a transmission path as receive data and storing the receive data received by the sending/receiving means.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to temporarily store the received data in the receive-data buffer so that the data can be processed by the

receiving circuit. The transmission and receiving circuits are used to transmit the data on the transmission medium and receive the send data from the transmission medium respectively.

Iseya also does not explicitly teach calculating an expected ECC for the data sequence having each piece of unit data and the expected ID in the receive data; comparing the ECC and the expected ECC in the receive data and issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same.

However Fredrickson in an analogous art teaches that error detection and correction techniques typically rely on some form of appended redundancy information to protect data blocks from errors during transmission through a noisy communication or recording channel. This appended redundancy is generated from, and thus dependent upon, the precise bit pattern that forms the data block to be protected. The integrity of the data at a receiving end is checked by regenerating the redundancy from the received data block (using the same coding algorithm used to generate the redundancy at the transmission end) and then comparing the regenerated redundancy with the originally appended redundancy. After this comparison, if data errors are determined to be present, a request can be made to re-transmit or re-read the data (col. 1, lines 26-40, Fredrickson).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Fredrickson by including an additional step of calculating an expected ECC for the data sequence having each piece of unit data and the expected ID in the receive data; comparing the ECC and the expected ECC in the receive data and issuing a resend request including the expected ID to the sending unit in the case where the ECC and the expected ECC in the receive data are not the same.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect data transmission errors in the receive data and retransmit the data if an error is detected.

Iseya also does not explicitly teach a computer program for driving a receiving computer to execute steps in a transmission data loss detection system.

However Sitterley in an analogous art teaches the computer program instructions may be executed by a processor to cause a series of operational steps to be performed by the processor to produce a computer implemented process such that the instructions which execute on the processor provide steps for implementing the functions specified in the flowchart block or blocks (col. 7, lines 15-20, Sitterley). Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify Iseya's patent with the teachings of Sitterley by including an additional step of using a computer program for driving a receiving computer to execute steps in a transmission data loss detection system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to execute the process steps faster and accurately.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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